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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,851	06/19/2003	Philip B. James-Roxby	X-1279 US	8477

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,851	JAMES-ROXBY ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,4-6 and 8-12* is/are allowed.

6)☒ Claim(s) *13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 April 2006 has been entered.

Status of Claims

2. Claims 1-2, 4-6, 8-13, 15-20 are pending in the Application.

Claims 1, 6, 13, 15 and 16 have been amended.

Claims 3, 7 and 14 have been canceled.

Claims 13 and 15-20 are rejected.

Claims 1-2, 4-6 and 8-12 are allowable.

Response to Amendment

3. Applicant's amendments and arguments filed on 2 March 2006 in response to the office action mailed on 28 December 2005 have been fully considered, but they are not persuasive (namely claims 13 and 15). Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address

the amendments. Additionally, the amendments and arguments with respect to claim 16 are moot in view of the new grounds of rejection necessitated by amendment.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 13, 15 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Song (US Patent 5,321,825).

As for claims 13 and 15, Song discloses a system and an apparatus for processing data stored in a memory shared among a plurality of processors, comprising:

a memory (Fig. 1, element 16);

and an integrated circuit including:

a semaphore circuit associated with a first portion of the memory, the semaphore circuit coupled to a bus shared by each of the plurality of processors (Fig. 1, element 62, the ULB lock field contains a bit which is used to indicate if the processor is permitted to access the critical section of the memory, which is further connected to the bus (element 18) -- col.4, lines 60-67. Note the buffer which contains the bit used as a semaphore in Song's

teachings can be part of integrated circuit common with the processors, therefore it itself must contain logic (i.e. circuitry) and can not be limited to a strictly software implementation – col. 9, lines 41-47);

means for storing tasks in the first portion of the memory, the tasks respectively related to data segments stored in a second portion of the memory (col. 5, lines 5-11, data operands are stored in the lock space (e.g. (element 162 of Fig. 2) which accessed by the instructions stored in the critical memory space);

means for controlling access among the plurality of processors to the first portion of the memory in response to a state of the semaphore circuit (col. 7, lines 11-15 -- when a processor accesses the critical section of the memory, all remaining processors are locked out);

means for executing a task to process a data segment in response to a processor of the plurality of processors gaining acçess to the first portion of the memory (col. 5, lines 4-11 -- the processor will execute instructions from the critical section of the memory which access data operands from the lock space memory once permission is granted through the LUB lock field); and

wherein each of the processors is coupled to a corresponding unshared memory (referring to Fig. 1, Song teaches

each of the processors as being coupled to a unique lock buffer (processor (12) is associated with buffer (28), likewise processor (14) with buffer (30)). These buffers are used to store information indicative of the state of the shared memory, and each of these buffers is used solely by its respective processor – col. 4, lines 30-51.

As for claim 20, Song discloses the system of claim 15, wherein the means for controlling comprises:

allowing one of the plurality of processors to access the first portion of the memory responsive to the semaphore having a first state value (col. 8, lines 49-55 – processor (element 12) is permitted to execute within the critical section as it is set to 0); and

blocking access to all of the plurality of processors to the first portion of the memory responsive to the semaphore having a second state value (col. 8, lines 53-57 – the other processors are blocked as the control bit used to determine their access control has been set to 1 (col. 8, lines 45-50)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song (US Patent 5,321,825) in further view of Trimberger (US Patent 6,573,748 B1) in further view of Carroll et al. (US Patent 4,322,846), hereinafter Carroll.

As for claims 16 and 18, though Song teaches all the elements of claim 15 (as described above), and his system as being integrated together within a single integrated circuit (hereinafter IC) in col. 9, lines 41-46, he fails to further define the IC as a programmable logic device, which is configured using programmable logic blocks.

Trimberger however discloses a programmable logic device, which is configurable (i.e. used as a processor in col. 1, lines 59-61) to increase the chip's versatility. Trimberger's programmable logic device (hereinafter PLD) utilizes an array of programmable logic blocks for the purposes of configuring the device (col. 1, lines 14-21). As Trimberger discloses, a PLD has many advantages because they are less expensive, and require less time to implement than semi-custom and fully custom ICs.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Song to allow further define his IC as an PLD IC in order to capitalize on the programmable features as disclosed by Trimberger. As taught by Trimberger, the increased programmability would help Song realize both decrease cost and implementation time.

Additionally, though Song teaches each of the processors as being coupled to an unshared memory (Fig. 1), he fails to specifically teach these memories as including Block RAMs as recited by Applicant.

Carroll however teaches a self-evaluation system for determining the operational integrity of a data processing system, which specifically discloses the use of Block RAM (BRAM) devices to store data (Fig. 3, element 61 – col. 6, lines 52-62).

It would have been obvious to one of ordinary skill in the art for Song to incorporate Carroll's self-evaluation system into his own processing system for providing critical section access. By doing so, Song would be able to increase the efficiency in which malfunctions in his own system could be diagnosed and corrected, and further provide a test system in which possible malfunctions of components within his own system could be identified – col. 2, lines 9-16.

As for claim 17, Song discloses each of the unique processors as being embedded within the IC (col. 9, lines 41-44).

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Song (US Patent 5,321,825), Trimberger (US Patent 6,573,748 B1), and Carroll (US Patent 4,322,846), as applied to claim 16 above, and further in view of Aucsmith et al. (US Patent 6,243,793 B1), hereinafter Aucsmith.

As for claim 19, though Song teaches all the limitations of claim 15 (including each of his processors as having its own unshared memory - referring to the rejection set forth above for claim 15), he fails to teach providing an

additional memory respectively to each of the plurality of processors. Aucsmith teaches a system for arbitrating access to a shared memory area which contains an additional memory, capable of storing program data to be executed by the processors (Fig. 2, element 103 illustrates a mass storage device that is connected to each of the two processors – col. 4, lines 12-18 the mass storage device provides information and data to the external memory which is used by the processors (i.e. element 104 in Fig. 2)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Song to further add an external memory to his processing system. By doing so, his system would benefit from additional storage area used to help coordinate memory access between the processors necessary to allow a plurality of processors operate on a shared memory as taught Aucsmith (col. 1, lines 15-21).

Response to Arguments

7. Applicant's arguments with respect to claims 13 and 15 have been considered, but they are not persuasive. More specifically, Applicant asserts Song teaches neither "each of the processors [as being] coupled to a corresponding unshared memory", nor "each of the processors ha[ving] its own unshared memory". Examiner finds these contentions not persuasive. Referring to Fig. 1, Song teaches each of the processors as being coupled to a unique lock buffer (processor (12) is associated with buffer (28), likewise processor (14) with buffer (30)). These buffers are used to store information

indicative of the state of the shared memory, and each of these buffers is used solely by its respective processor, hence it is unshared (emphasis added) – col. 4, lines 30-51.

8. Applicant's arguments with respect to claim 16 have been considered but are moot in view of the new ground(s) of rejection as discussed *supra*.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

5/17/06

CEW

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER